IN THE CLAIMS:

Please cancel Claims 34 - 45 without prejudice, and amend Claims 1- 3, 12 - 14, and 24 - 26 as follows:

1. (Currently Amended) A semiconductor processing chamber ~~having at least one interior surface comprising~~ , where a surface of previously unroughened aluminum or aluminum alloy has been roughened using electrochemical treatment of said ~~electrochemically roughened aluminum or aluminum alloy,~~ surface ~~wherein~~ in a manner such that said ~~electrochemically roughened~~ surface has the appearance of rolling hills and valleys, when magnified.

2. (Currently Amended) The semiconductor processing chamber of Claim 1, wherein said at least one interior surface has a surface roughness ranging from about 100 μm Ra to about 200 μm Ra.

3. (Currently Amended) The semiconductor processing chamber of Claim 2, wherein said surface roughness ranges from about 110 μm Ra to about 160 μm Ra.

4. (Cancelled)

5. (Previously Presented) The semiconductor processing chamber of Claim 1, wherein the height of said hills ranges from about 8 μm to about 25 μm.

6. (Previously Presented) The semiconductor processing chamber of Claim 1 or Claim 5, wherein the distance between the center of one hill and the center of an adjacent hill ranges from about 30 μm to about 100 μm.

7. (Original) The semiconductor processing chamber of Claim 1, wherein said electrochemically roughened aluminum or aluminum alloy surface underlies a coating selected from the group consisting of an anodized coating, a flame spray-deposited aluminum oxide coating, a ceramic coating, and an anodized coating having a ceramic coating applied thereover.

8. (Previously Presented) The semiconductor processing chamber of Claim 1 or Claim 7, wherein byproducts generated during an etch process or a deposition process adhere to said electrochemically roughened aluminum or aluminum alloy surface or to said coating overlying said electrochemically roughened aluminum or aluminum alloy surface.

9. (Original) The semiconductor processing chamber of Claim 1, wherein said semiconductor processing chamber is selected from the group consisting of an etch chamber and a deposition chamber.

10. (Original) The semiconductor processing chamber of Claim 9, wherein said semiconductor processing chamber is an etch chamber which is used for etching a material selected from the group consisting of a dielectric material, a metal, and polysilicon.

11. (Original) The semiconductor processing chamber of Claim 9, wherein said semiconductor processing chamber is an etch chamber, and wherein fluorine and carbon from an etch process react to form a polymer which adheres to said electrochemically roughened aluminum surface.

12. (Currently Amended) A processing component for use within a semiconductor processing chamber, wherein at least one surface of said processing component comprises aluminum or an aluminum alloy, and wherein ~~said processing component has~~ at least one

~~electrochemically roughened~~ previously unroughened aluminum or aluminum alloy surface has been ~~, wherein said at least one~~ electrochemically roughened so that said at least one aluminum or aluminum alloy surface has the appearance of rolling hills and valleys, when magnified.

13. (Currently Amended) The processing component of Claim 12, wherein said electrochemically roughened aluminum or aluminum alloy surface has a surface roughness ranging from about 100 μm Ra to about 200 μm Ra.

14. (Currently Amended) The processing component of Claim 13, wherein said surface roughness ranges from about 110 μm Ra to about 160 μm Ra.

15. (Cancelled)

16. (Previously Presented) The processing component of Claim 12, wherein the height of said hills ranges from about 8 μm to about 25 μm.

17. (Previously Presented) The processing component of Claim 12 or Claim 16, wherein the distance between the center of one hill and the center of an adjacent hill ranges from about 30 μm to about 100 μm.

18. (Original) The processing component of Claim 12, wherein said electrochemically roughened aluminum or aluminum alloy surface underlies a coating selected from the group consisting of an anodized coating, a flame spray-deposited aluminum oxide coating, a ceramic coating, and an anodized coating having a ceramic coating applied thereover.

19. (Previously Presented) The processing component of Claim 12 or Claim 18, wherein byproducts generated during an etch process or a deposition process adhere to said electrochemically roughened aluminum or aluminum alloy surface or to said coating overlying said electrochemically roughened aluminum or aluminum alloy surface.

20. (Original) The processing component of Claim 12, wherein said processing component is used within a semiconductor processing chamber selected from the group consisting of an etch chamber and a deposition chamber.

21. (Original) The processing component of Claim 20, wherein said semiconductor processing chamber is an etch chamber which is used for etching a material selected from the group consisting of a dielectric material, a metal, and polysilicon.

22. (Original) The processing component of Claim 20, wherein said semiconductor processing chamber is an etch chamber, and wherein fluorine and carbon from an etch process react to form a polymer which adheres to said electrochemically roughened surface.

23. (Original) The processing component of Claim 12, wherein said processing component is selected from the group consisting of: a wall liner, a cathode liner, a slit valve door, a slit valve liner, a buffer insert, and a gas distribution plate.

24. (Currently Amended) A semiconductor processing apparatus surface, wherein said surface ~~comprises~~ is a previously unroughened aluminum or aluminum alloy surface which has been electrochemically roughened ~~aluminum or aluminum alloy, wherein~~ so that said surface has the appearance of rolling hills and valleys, when magnified.

25. (Currently Amended) The semiconductor processing apparatus surface of Claim 24, wherein said surface has a surface roughness ranging from about 100 μm Ra to about 200 μm Ra.

26. (Currently Amended) The semiconductor processing apparatus surface of Claim 25, wherein said surface roughness ranges from about 110 μm Ra to about 160 μm Ra.

27. (Cancelled)

28. (Previously Presented) The semiconductor processing apparatus surface of Claim 24, wherein the height of said hills ranges from about 8 μm to about 25 μm.

29. (Previously Presented) The semiconductor processing apparatus surface of Claim 24 or Claim 28, wherein the distance between the center of one hill and the center of an adjacent hill ranges from about 30 μm to about 100 μm.

30. (Original) The semiconductor processing apparatus surface of Claim 24, wherein said surface underlies a coating selected from the group consisting of an anodized coating, a flame spray-deposited aluminum oxide coating, a ceramic coating, and an anodized coating having a ceramic coating applied thereover.

31. (Previously Presented) The semiconductor processing apparatus surface of Claim 24 or Claim 30, wherein byproducts generated during an etch process or a deposition process adhere to said electrochemically roughened surface or to said coating overlying said electrochemically roughened surface.

32. (Original) The semiconductor processing apparatus surface of Claim 31, wherein fluorine and carbon from an etch process react to form a polymer which adheres to said surface.

33. (Original) The semiconductor processing apparatus surface of Claim 24, wherein said surface is present on an apparatus component selected from the group consisting of: a wall liner, a cathode liner, a slit valve door, a slit valve liner, a buffer insert, and a gas distribution plate.

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)

39. (Cancelled)

40. (Cancelled)

41. (Cancelled)

42. (Cancelled)

43. (Cancelled)

44. (Cancelled)

45. (Cancelled)